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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,798	08/19/2002	Hsiu-O Hsu	9051-US-PA	4096
31561	7590	02/23/2004	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE			CHOI, JACOB Y	
7 FLOOR-1, NO. 100			ART UNIT	PAPER NUMBER
ROOSEVELT ROAD, SECTION 2			2875	
TAIPEI, 100				
TAIWAN				
DATE MAILED: 02/23/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

TM

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/064,798	HSU, HSIU-O	
	Examiner	Art Unit	
	Jacob Y Choi	2875	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 16 December 2003.

2a) This action is **FINAL**.                                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1 and 3-6 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1 and 3-6 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 08/19/2002 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.

4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Drawings***

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the forested surface, the first region includes a first ejected material, and the second region includes a second ejected material must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Any structural detail that is of sufficient importance to be described should be shown in the drawing (Ex parte Good, 1911 C.D. 43, 164 O.G. 739 (Comm'r Pat. 1911).) See MPEP 608.02.

Note: amendment to the claims now requires "*a distance from a bottom of the light-emitting diodes to the printed circuit board is larger than a distance from a top of the reflection boards to the printed circuit board*"

### ***Claim Objections***

2. Claim 1 is objected to because of the following informalities: grammatical error appears in line 6 "*wherein the a surface of the light-collecting column*". Appropriate correction is required.

***Specification***

3. The disclosure is objected to because of the following informalities: the speciation has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification. Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (USPN 5,639,158) in view of Shoenfeld (USPN 6,364,505).

Regarding claim 1, Sato discloses a printed circuit board (1), on which a plurality of electrodes are formed (2), a plurality of light-emitting diodes (2) disposed on the printed circuit board and electrically coupled together, and at least one light-collecting column (3), disposed over the printed circuit board (1), and covering the light-emitting

diodes (2), wherein the a surface of the light-collecting column has a plurality of first regions (4a shown in figure 1A) and a plurality of second regions (4b shown in figure 1C), the first regions and the second regions are arranged alternatively on the light-collecting column, wherein a transmittance for the first regions is smaller than a transmittance for the second regions (figures 2B & 2C), and the first regions are located above the light emitting diodes, wherein the first region is metal such as aluminum (but ***not limited to aluminum as long as it conforms to the subject*** ... where a long light-transmitting plate (3) is being ***glass*** or plastic providing on the LED-array for leading output light; column 2, lines 45-50 & column 3, lines 45-50).

Note: the word frosted is defined as a cover (glass, for example) with a roughened or speckled decorative surface

Sato discloses the claimed invention except the specifics of a frosted surface that one in ordinary skill in the art might conceive as. Shoenfeld teaches that it is known to utilize frosted front diffuser (24) with varying intensity frosting (figures 1, 2, & 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use modification in Sato as taught by Shoenfeld in order to utilize well known a front diffuser that is formed of a glass plate that is etched or frosted (column 4, lines 45-55) to diffuse & vary intensity of LED light array(s).

6. Claims 3, 4, & 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (USPN 5,639,158).

Regarding claim 3, Sato discloses a printed circuit board (1), on which a plurality of electrodes are formed (2), a plurality of light-emitting diodes (2) disposed on the printed circuit board and electrically coupled together, and at least one light-collecting column (3), disposed over the printed circuit board (1), and covering the light-emitting diodes (2), wherein the a surface of the light-collecting column has a plurality of first regions (4a shown in figure 1A) and a plurality of second regions (4b shown in figure 1C), the first regions and the second regions are arranged alternatively on the light-collecting column, wherein a transmittance for the first regions is smaller than a transmittance for the second regions (figures 2B & 2C), and the first regions are located above the light emitting diodes, wherein the first region includes a first ejected material (4a) and the second region includes a second ejected material (4b). Sato discloses the claimed invention except for specific materials that is ejected to the first and second regions. It would have been obvious to one having ordinary skill in the art at the time the invention was made to eject known material as Sato teaches (*not limited to aluminum as long as it conforms to the subject* ... where a long light-transmitting plate (3) is being **glass** or plastic providing on the LED-array for leading output light; column 2, lines 45-50 & column 3, lines 45-50), since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 146.

Regarding claim 4, Sato discloses a printed circuit board (1), on which a plurality of electrodes are formed (LED / inherent), a plurality of light-emitting diodes (2) disposed on the printed circuit board (1) and electrically coupled together, at least one

light-collecting column (3), disposed over the printed circuit board, and covering the light-emitting diodes, and a plurality of reflection boards (4a & 4b), disposed between the light-emitting diodes and the printed circuit board, wherein a distance from a bottom of the light-emitting diodes to the printed circuit board is larger than a distance from a top of the reflection board to the printed circuit board, so as to enhance a brightness at a region between the light emitting diodes (figures 2B & 2C). Sato discloses the claimed invention except for specific distance range of the light-emitting diodes to the printed circuit board and the top of the reflection boards to the printed circuit board. It would have been obvious to one having ordinary skill in the art at the time the invention was made to specify optimum distance range of the mentioned elements, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 6, Sato discloses the claimed invention, explained above. In addition, Sato discloses he reflection boards are used to reflect an incident light to region between the light emitting diodes.

7. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (USPN 5,580,156).

Regarding claim 4, Suzuki et al. discloses a printed circuit board (11), on which a plurality of electrodes are formed (LED / inherent), a plurality of light-emitting diodes (13) disposed on the printed circuit board (11) and electrically coupled together, at least

one light-collecting column (4), disposed over the printed circuit board, and covering the light-emitting diodes (13), and a plurality of reflection boards (22), disposed between the light-emitting diodes (13) and the printed circuit board (11), wherein a distance from a bottom of the light-emitting diodes to the printed circuit board is larger than a distance from a top of the reflection boards to the printed circuit board, so as to enhance a brightness at a region between the light emitting diodes (figures 6-8). Suzuki et al. discloses the claimed invention except for specific distance range of the light-emitting diodes to the printed circuit board and the top of the reflection boards to the printed circuit board. It would have been obvious to one having ordinary skill in the art at the time the invention was made to specify optimum distance range of the mentioned elements, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 5, Suzuki et al. discloses each of the reflection boards comprise a plurality of reflection surfaces (figures 4 & 5).

Regarding claim 6, Suzuki et al. discloses the reflection boards are used to reflect an incident light to region between the light emitting diodes.

8. Claims 1, & 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda (USPN 6,533,429).

Regarding claim 1, Yoneda discloses a printed circuit board (5), on which a plurality of electrodes are formed, a plurality of light-emitting diodes (4) disposed on the

printed circuit board and electrically coupled together, and at least one light-collecting column (6), disposed over the printed circuit board, and covering the light-emitting diodes, wherein the surface of the light-collecting column has a plurality of first regions (6A) and a plurality of second regions (7), the first regions and the second regions are arranged alternatively (side vs. face) on the light-collecting column, wherein a transmittance for the first regions (column 5, lines 15-35) is smaller than a transmittance for the second regions (reflective), and the first regions are located below (however figures 11 & 12 maybe viewed upside down to show the first regions are located above the light emitting diodes) the light-emitting diodes, wherein the first regions is frosted surface (column 5, lines 15-35). Yoneda discloses the claimed invention except for specific arrangement of the first regions. It would have been obvious to one having ordinary skill in the art at the time the invention was made to rearrange or simply view the teachings of Yoneda upside down, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

Regarding claim 3, Yoneda discloses a printed circuit board (5), on which a plurality of electrodes are formed, a plurality of light-emitting diodes (4) disposed on the printed circuit board and electrically coupled together, and at least one light-collecting column (6), disposed over the printed circuit board, and covering the light-emitting diodes, wherein the surface of the light-collecting column has a plurality of first regions (6A) and a plurality of second regions (7), the first regions and the second regions are arranged alternatively (side vs. face) on the light-collecting column, wherein a transmittance for the first regions (column 5, lines 15-35) is smaller than a transmittance

for the second regions (reflective), and the first regions are located below (however figures 11 & 12 maybe viewed upside down to show the first regions are located above the light emitting diodes) the light-emitting diodes, wherein the first region includes a first ejected material and the second region includes a second ejected material.

Yoneda discloses specific details of materials that are ejected to the first and second regions. It would have been obvious to one having ordinary skill in the art at the time the invention was made to eject known material as Yoneda teaches (column 5, lines 15-35; it is also possible to structure a frosted glass surface by providing minute concavities and convexities on the exit faces 6A ... in order to attain the advantage of obtaining a further even brightness as a result of the light being dispersed ... etc), since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 146.

Regarding claim 4, Yoneda discloses a printed circuit board, on which a plurality of electrodes are formed, a plurality of light-emitting diodes disposed on the printed circuit board, and covering the light-emitting diodes, and a plurality of reflection boards, disposed between the light-emitting diodes and the printed circuit board, wherein a distance from a bottom of the light-emitting diodes to the printed circuit board is larger than a distance from a top of the reflection boards to the printed circuit board, so as to enhance a brightness at a region between the light emitting diodes. Yoneda discloses the claimed invention except for specific distance range of the light-emitting diodes to the printed circuit board and the top of the reflection boards to the printed circuit board.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to specify optimum distance range of the mentioned elements, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 5, Yoneda discloses the claimed invention, explained above. IN addition, Yoneda discloses each of the reflection boards comprises a plurality of reflection surfaces.

Regarding claim 6, Yoneda discloses the claimed invention, explained above. IN addition, Yoneda discloses the reflection boards are used to reflect an incident light to a region between the light-emitting diodes.

#### ***Response to Arguments***

9. The amendment filed 08/28/2003 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: amendment to the claims now requires "*a distance from a bottom of the light-emitting diodes to the printed circuit board is larger than a distance from a top of the reflection boards to the printed circuit board*"

Applicant is required to cancel the new matter in the reply to this Office Action.

The proposed amendment will not be entered because they raise the issue of new matter.

Applicant's arguments with respect to claims 1, 3-6 have been considered but are moot in view of the new ground(s) of rejection.

Claims in a pending application should be given their broadest reasonable interpretation. *In re Pearson*, 181 USPQ 641 (1974).

Note: especially the word "frost"

### ***Conclusion***

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

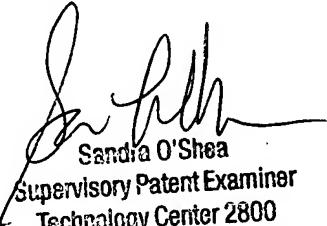
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Y Choi whose telephone number is (571) 272-2367. The examiner can normally be reached on Monday-Friday (10:00-7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sandra O'Shea can be reached on (571) 272-2378. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JC



Sandra O'Shea  
Supervisory Patent Examiner  
Technology Center 2800